National Semiconductor

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LM4308
Mobile Pixel Link Two (MPL-2) – 18-bit CPU Display Interface Master/Slave

General Description

The LM4308 device adapts a 18-bit CPU style display interfaces to a MPL-2 SLVS differential serial link for displays. Two chip selects support a main and sub display up to and beyond 640 x 480 pixels. A mode pin configures the device as a Master (MST) or Slave (SLV). Both WRITE and READ operations are supported. CPU interface widths below 18-bits are supported by tieing unused inputs to a static level.

The differential line drivers and receivers conform to the JEDEC SLVS Standard. When noise is picked up as common-mode, it is rejected by the receivers. This is further enhanced with the 50 Ohm output impedance of the drivers. The 100 Ohm termination is integrated into the receivers.

Data integrity is insured with a 5-bit CRC field. CRC checking is done for both WRITE and READ operations. An Error (ERR) pin reports the occurrence of an error. A Write Only mode is also provided.

The interconnect is reduced from 23 signals to only 4 active signals with the LM4308 chipset easing flex interconnect design, size constraints and cost.

A low power sleep state entered when the PD* inputs are driven low.

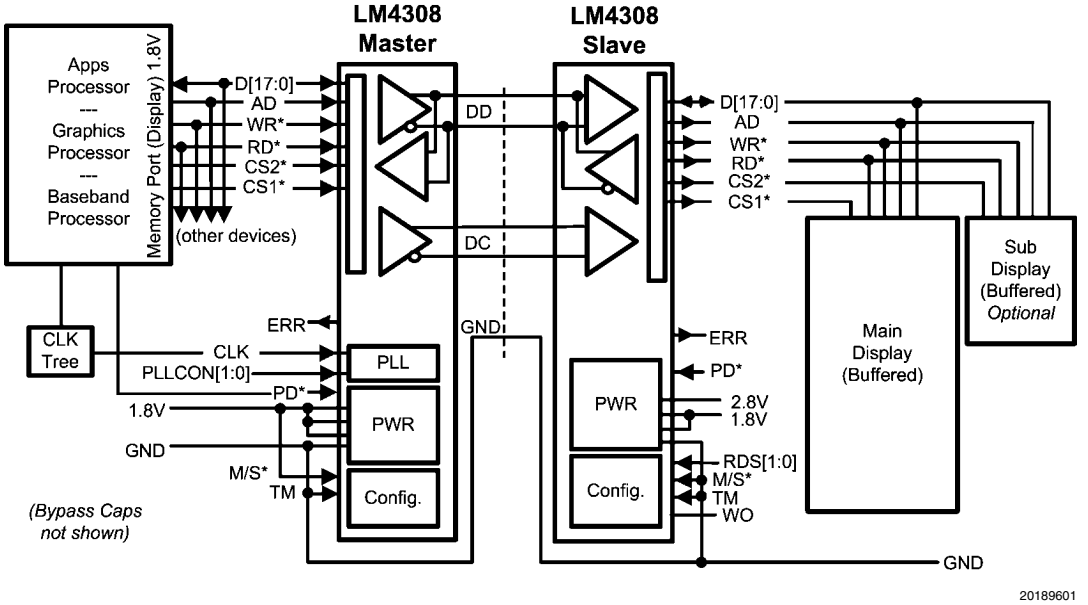
Features

- 18-bit i80 CPU Display Interface
- Supports up to 640 x 480 VGA formats
- Differential SLVS Interface
- Dual displays supported
- WRITE and READ operations supported
- Robust Differential Physical Layer
- 400mVpp differential signal swing
- Internal 100 Ω Termination Resistor
- Low Power Consumption
- 5-bit CRC for data integrity
- Level translation between host and display
- Low Power sleep state
- 3.3V Tolerant Master Clock Input regardless of V_{DDIO}
- Fast Start Up Time - 1k CLK cycles
- 1.6V to 2.0V core / analog supply voltage
- 1.6V to 3.0V I/O supply voltage range

System Benefits

- Small Interface
- Low Power
- Low EMI
- Intrinsic Level Translation

Typical Application Diagram



Pin Descriptions

Pin Name	No. of Pads uArray	No. of Pins LLP	I/O, Type	Description	
				CPU Master (MST)	CPU Slave (SLV)
SLVS SERIAL BUS PINS					
DDP	1	1	IO, slvs	Differential Data - Positive, Transceiver	
DDN	1	1	IO, slvs	Differential Data - Negative, Transceiver	
DCP	1	1	O, I, slvs	Differential Clock - Positive, Line Driver	Differential Clock - Positive, Receiver
DCN	1	1	O, I, slvs	Differential Clock - Negative, Line Driver	Differential Clock - Clock, Receiver
CONFIGURATION/PARALLEL BUS PINS					
M/S*	1	1	I, LVCMOS	High for Master	Low for Slave
TM	1	1	I, LVCMOS	Test Mode Control Input **Tie Low** L = Normal H = Test Mode (factory test only)	
PLLCON [1:0]	2	2	I, LVCMOS	PLL Multiplier Input Pins See *PLLCON[1:0] - PLL Multiplier Settings*	NA
RDS[1:0]	2	2	I, LVCMOS	NA	Receiver Drive Strength Control Input Pins, See *RDS[1:0] - Receiver Output Drive Strength*
ERR	1	1	O, LVCMOS	Error Output Signal Indicates a CRC error on the READ Payload	Error Output Signal Reports a CRC error was detected on the WRITE Payload
WO	1	1	I, LVCMOS	NA	WRITE Only Control Input L = Writes and reads enabled H = Write Only
CLOCK / POWER DOWN SIGNALS					
CLK	1	1	I, LVCMOS	CLK Input Input is 3.3V Tolerant regardless of V_{DDIO}	NA
PD*	1	1	I, LVCMOS	Power Down Input, L = Powered down, Low Power SLEEP state H = active state	
PARALLEL INTERFACE SIGNALS					
D[17:0]	18	18	IO, LVCMOS	CPU Data Bus Inputs / Outputs	CPU Data Bus Outputs / Inputs
CS1* CS2*	2	2	I, O, LVCMOS	Chip Select Input Pins Only one CS is allowed to be Low at a time.	Chip Select Output Pins
RD*	1	1	I, O, LVCMOS	Read Enable Input, active Low	Read Enable Output, active Low
WR*	1	1	I, O, LVCMOS	Write Enable Input, active Low	Write Enable Output, active Low
AD	1	1	I, O, LVCMOS	Address / Data selector input	Address / Data selector output

Pin Name	No. of Pads uArray	No. of Pins LLP	I/O, Type	Description	
				CPU Master (MST)	CPU Slave (SLV)
POWER/GROUND PINS					
V_{DDA}	1	1	Power	Power Supply Pin for the PLL (MST) and SLVS Interface. 1.6V to 2.0V	
V_{SSA}	1	1	Ground	Ground Pin for the PLL (MST) and SLVS Interface.	
V_{DD}	1	1	Power	Power Supply Pin for the digital core. 1.6V to 2.0V	
V_{SS}	1	*	Ground	Ground Pin for the digital core.	
V_{DDIO}	2	2	Power	Power Supply Pin for the parallel interface I/Os. 1.6V to 3.0V	
V_{SSIO}	9	*	Ground	Ground Pin for the parallel interface I/Os. For the LLP Package, VSSIO and VSS	
DAP	NA	* 1		Connect to Ground - LLP Package Ground pin for V_{SSIO} and V_{SS}	

Note:
I = Input, O = Output, IO = Input/Output. Do not float input pins.

PLLCON[1:0] - PLL Multiplier Settings

PLLCON1	PLLCON0	Multiplier
L	L	8X
L	H	10X
H	L	12X
H	H	Reserved

RDS[1:0] - Receiver Output Drive Strength

RDS1	RDS0	Result
L	L	Use with High V_{DDIO} operation
L	H	Increased drive on DATA, AD, and CS1*/CS2* outputs
H	L	Increased drive on WR* and RD*
H	H	All outputs, use for Low V_{DDIO}, Increased drive strength on all outputs

Ordering Information

NSID	Package Type	Package ID
LM4308GR	49L MicroArray, 4.0 X 4.0 X 1.0 mm, 0.5 mm pitch	GRA49A
LM4308SQ	40L LLP, 5.0 X 5.0 X 0.8 mm, 0.4 mm pitch	SQF40A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DDA})	−0.3V to +2.2V
Supply Voltage (V_{DD})	−0.3V to +2.2V
Supply Voltage (V_{DDIO})	−0.3V to +3.6V
LVCMOS Input/Output Voltage	−0.3V to (V_{DDIO} +0.3V)
CLK LVCMOS Input Voltage	−0.3V to +3.3V
SLVS Input/Output Voltage	−0.3V to V_{DDA}
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
ESD Ratings:	
HBM, 1.5 kΩ, 100 pF	≥±2 kV
EIAJ, 0Ω, 200 pF	≥±200V
Maximum Package Power Dissipation Capacity at 25°C	
GRA Package	2.75 W
Derate GRA Package above 25°C	22 mW/°C
SQF Package	3.43 W
Derate SQF Package above 25°C	27 mW/°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage				
V_{DDA} to V_{SSA} and V_{DD} to V_{SS}	1.6	1.8	2.0	V
V_{DDIO} to V_{SSIO}	1.6		3.0	V
Clock Frequency	9.6		30	MHz
DC (Serial) Clock Frequency	76.8		240	MHz
Ambient Temperature	−40	25	85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
SLVS							
V_{OD}	Differential Output Voltage		100 Ω Load	140	200	270	mV
ΔV_{OD}	Differential Output Voltage Match	(Note 9)		-10	0	10	mV
V_{OS}	Driver Offset Voltage			150	200	250	mV
ΔV_{OS}	Driver Offset Voltage Match	(Note 9)		-5	0	5	mV
R_{OUT}	Driver Output Impedance		High Output		50		Ω
			Low Output		50		Ω
V_{OH}	High Level Output Voltage	(Diff. Mode)				360	mV
R_T	Receiver Differential Termination Resistor	DD (RX) Configuration or DC (SLV) (Note 8)		80	100	125	Ω
V_{IDH}	Differential Input High Threshold	RX, V_{CM} = 35mV, 200mV and 365mV (Note 9)			10	70	mV
V_{IDL}	Differential Input Low Threshold			−70	-10		mV
V_{CM}	Receiver Common Mode Input Range	RX with V_{ID} = |70mV|		35		365	mV

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVCMOS							
V_{IH}	Input Voltage High Level			0.7 V_{DDIO}		V_{DDIO}	V
V_{IL}	Input Voltage Low Level			GND		0.3 V_{DDIO}	V
V_{HY}	Input Hysteresis				160		mV
I_{IH}	Input Current High Level	LVCMOS Inputs	$V_{IN} = V_{DDIO}$	−1	0	+1	µA
		CLK Input	V_{IN} = 3.3V V_{DDIO} = 1.8V (Note 10)	0		+8	µA
		CLK Input	V_{IN} = 1.8V V_{DDIO} = 1.8V	−1	0	+1	µA
I_{IL}	Input Current Low Level			−1	0	+1	µA
V_{OH}	Output Voltage High Level	I_{OH} = −2 mA RDS = H V_{DD} = 1.6 V , V_{DDIO} = 2.0 V		0.75 V_{DDIO}		V_{DDIO}	V
		I_{OH} = −2 mA RDS = L V_{DD} = 2.0 V , V_{DDIO} = 3.0 V		0.8 V_{DDIO}		V_{DDIO}	V
V_{OL}	Output Voltage Low Level	I_{OL} = 2 mA RDS = H V_{DD} = 1.6V , V_{DDIO} = 2.0 V		V_{SSIO}		0.2 V_{DDIO}	V
		I_{OL} = 2 mA RDS = L V_{DD} = 2.0 V , V_{DDIO} = 3.0 V		V_{SSIO}		0.2 V_{DDIO}	V
SUPPLY CURRENT							
I_{DD}	Total Supply Current—Enabled Conditions: CLK = 30MHx (8X mode), DC = 240MHz, DD = 480Mbps Worse Case Data Pattern, constant WRITE	Master (Note 11)	V_{DDIO}			64	µA
			V_{DD}/V_{DDA}			18	mA
		Slave (Note 11)	V_{DDIO}			18	mA
			V_{DD}/V_{DDA}			7	mA
	Supply Current—Enabled Bus Idle (WR* = H)	Master	V_{DDIO}		10		µA
			V_{DD}/V_{DDA}		8.2		mA
		Slave	V_{DDIO}		>1		µA
			V_{DD}/V_{DDA}		2.9		mA
I_{DDZ}	Supply Current—Disable Power Down Modes	Master PD* = L, or CLK stop	V_{DDIO}			8	µA
			V_{DD}/V_{DDA}			9	µA
		Slave PD* = L, or Auto Sleep	V_{DDIO}			8	µA
			V_{DD}/V_{DDA}			9	µA
PD	Power Dissipation	25% Bus active	Master		15		mW
			Slave		6		mW
		Idle Bus	Master		14.8		mW
			Slave		5.2		mW
		QVGA (Note 5)	Master		195		µW
			Slave		8		µW
		PD*=L	Master		>0.1		µW
			Slave		>0.1		µW

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
PARALLEL BUS TIMING See also *Table 2* and *Figure 9*							
t_{SET}	Set Up Time	Master Input, WRITE		5			ns
t_{HOLD}	Hold Time			5			ns
t_{RISE}	Rise Time	RD* and WR* Slave Outputs(Note 4) C_L = 15 pF, *Figure 2*	V_{DDIO} = 1.6V RDS = H		7		ns
			V_{DDIO} = 3.0V RDS = L		7		ns
t_{FALL}	Fall Time		V_{DDIO} = 1.6V RDS = H		7		ns
			V_{DDIO} = 3.0V RDS = L		6		ns
SERIAL BUS TIMING							
t_{DVBC}	Data Valid before DC Clock	Master (Note 9)		26%		74%	UI
t_{DVAC}	Data Valid after DC Clock			26%		74%	UI
t_{Sset}	Serial Set Time	Slave (Note 8)		400			ps
t_{Shold}	Serial Hold Time			400			ps
t_T	Transition Time	Master	20% to 80%		200		ps
POWER UP TIMING							
t_a	DC ON High Delay	Link Start Up Sequence			128		CLK cycles
t_b	DC Low Delay				128		CLK cycles
t_c	DC Active Delay				504		CLK cycles
t_d	DD High Delay				128		CLK cycles
t_e	DD Low Delay				8		CLK cycles
t_f	DD Differential ON				128		CLK cycles
t_{SU}	Start Up Delay Includes PLL Lock Time	$t_a + t_b + t_c + t_d + t_e + t_f$			1,024		CLK cycles
POWER OFF TIMING							
t_O	Turn Off Delay	(Note 7)			0.1	2	µs

Recommended Input Timing Requirements

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MASTER REFERENCE CLOCK (CLK)						
f	Clock Frequency		9.6		30	MHz
t_{CP}	Clock Period		33.3		104.2	ns
CLK_{DC}	Clock Duty Cycle		30	50	70	%
t_T	Clock/Data Transition Times	(Rise or Fall, 10%–90%)(Note 6)	2	>2		ns
t_{CLKgap}	CLK Stop Gap		4			CLKcycles

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{DDIO} = 1.8V and V_{DD} = V_{DDA} = 1.8V and T_A = 25°C.

Note 3: Current into a device pin is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to Ground unless otherwise specified.

Note 4: Rise and Fall Time tested on the following pins only: WR* and RD*.

Note 5: Typical PD for QVGA application. Conditions: 1.8V, 25C, 19.2MHz CLK and 8X, 10% blanking, 1fps. Link is started up, 1 frame (240 x 320) is sent and link is powered down.

Note 6: Maximum transition time is a function of clock rate and should be less than 30% of the clock period to preserve signal quality.

Note 7: Guaranteed functionally by the I_{DDZ} parameter. See also *Figure 7*.

Note 8: Specification is guaranteed by design and is not tested in production.

Note 9: Specification is guaranteed by characterization and is not tested in production.

Note 10: When clock input is in overdrive (Vin = 3.3 V) and then stop clock is applied, it is recommended to set input clock to a low state.

Note 11: For IDD measurments a checkerboard pattern 2AAAA-15555 was used.

Timing Diagrams

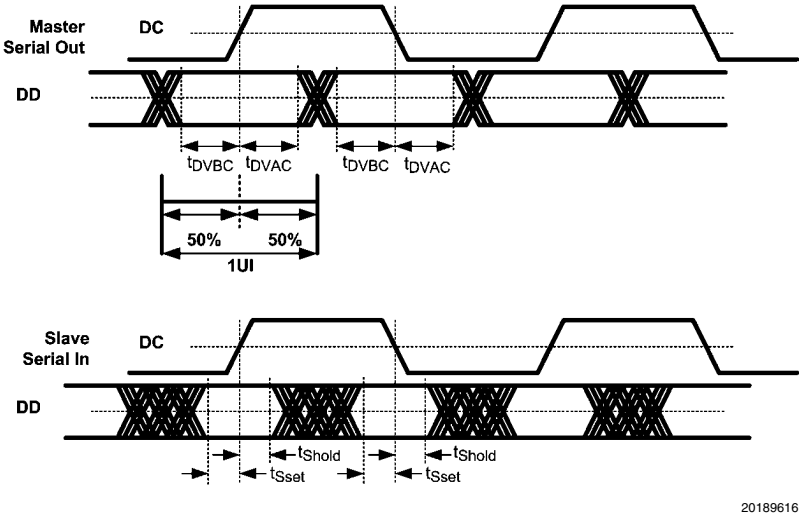


FIGURE 1. Serial Data Valid & Set/Hold Times

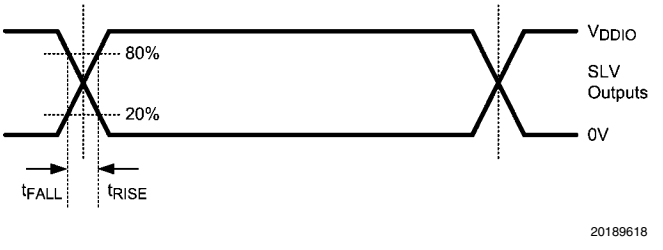


FIGURE 2. Slave Output Rise and Fall Time (WR* and RD*)

Functional Description

BUS OVERVIEW

The LM4308 is a Master (SER) / Slave (DES) configurable part that supports a 18-bit (or less) i80 CPU Display interface. Both WRITE and READ transactions are supported. The SLVS physical layer is purpose-built for an extremely low power and low EMI data transmission while requiring the fewest number of signal lines. No external line components are required, as termination is provided internal to the SLVS receiver. A maximum raw throughput of 480 Mbps (raw) is possible with this chipset. The SLVS interface is designed for use with 100Ω differential lines.

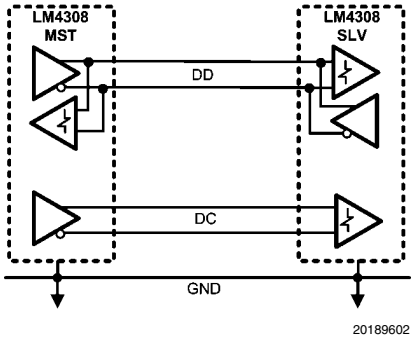


FIGURE 3. SLVS Point-to-Point Bus

SERIAL BUS TIMING

Data valid is relative to both edges for a CPU WRITE as shown in *Figure 4*. Data valid is specified as: Data Valid before Clock, Data Valid after Clock, and Skew between data lines should be less than 500ps.

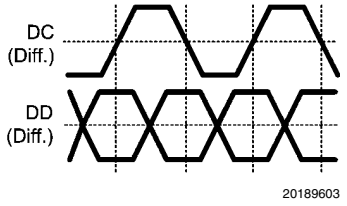


FIGURE 4. Serial Link Timing (WRITE)

Data is strobed out on the Rising edge by the Slave for a CPU READ as shown in *Figure 5*. The Master monitors for the start bit transition (High to Low) and then selects the best strobe to sample the incoming data on. This is done to account for the round trip delay of the interconnect and application data rate. Since READ data is sent on one edge only, the back channel rate (READ) is one quarter that of the WRITE rate.

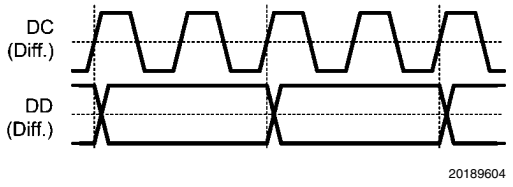


FIGURE 5. Serial Link Timing (READ)

SERIAL BUS PHASES

There are five bus phases on the serial bus. These are determined by the state of the DC and DD lines. The bus phases are shown in *Table 1*.

TABLE 1. Link Phases

Name		DC State	DD State	Phase Description	Pre-Phase	Post-Phase
OFF (O)		GND	GND	Link is Off	A, I or LU	LU
IDLE (I)		A	H	Idle, MD(s) = Logic Low	A or LU	A or O
ACTIVE (A), Write		A	X	Write Payloads	LU, A, or I	A, I, or O
ACTIVE, Read	Read Command	A	X (MST)	Read Command	A, or I	
	TA’	A	HUH	MD Turn Around	RC	RD
	Read Data	A	X (SLV)	Read Payload	TA’	TA"
	TA"	A	HUH	MD Turn Around	RD	I
LINK-UP (LU)	Master	*	*	Start Up	O	A, I, or O

Notes on DC/DD Line State:
0 = no current (off)

SERIAL BUS START UP TIMING

The DC and DD lines are held at a LVCMOS Low state in the Sleep state (PD* = L). When the PD* signal is switched to a High state the DC lines are pulsed. Next the DC lines are driven to the differential levels and the clock signal is active. The DD lines are then pulsed from a LVCMOS Low state, then driven to a valid differential static High state. Data transmission (WRITE) starts with a valid Low start bit on the DD signal.

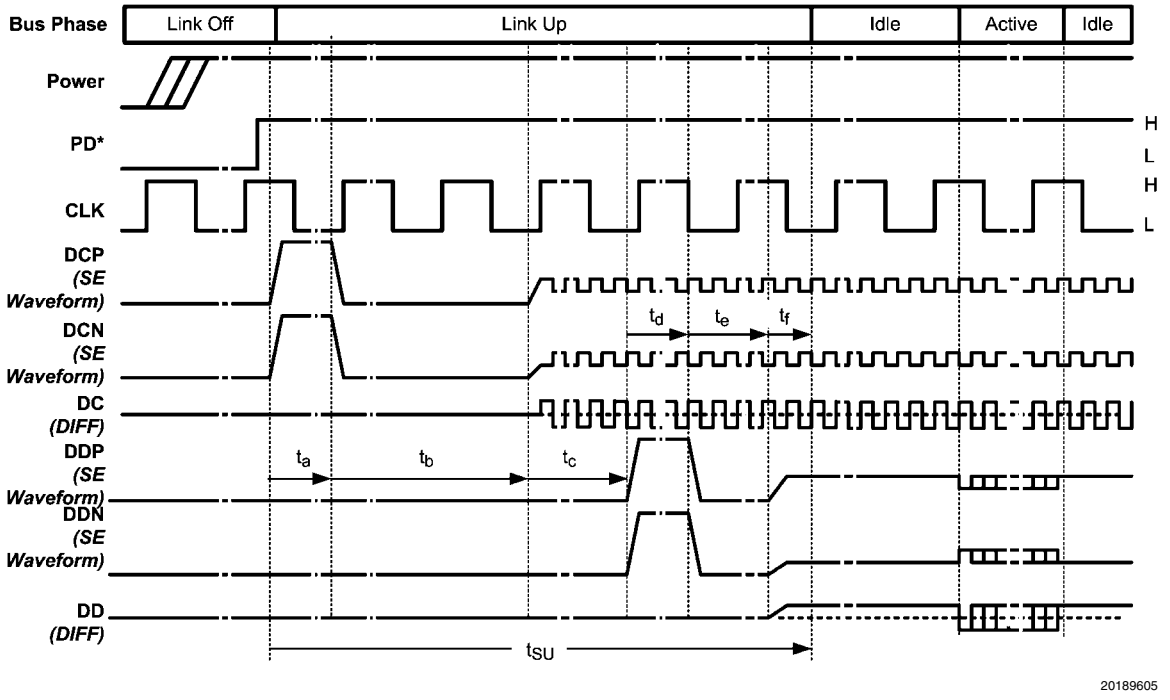


FIGURE 6. Serial Bus Power Up Timing

Actual start up time is clock rate dependant. The 1024 CLK counter encompasses both the SLVS start up delay and PLL Lock Time. At 19.2MHz operation, the link is ready for transmission after only 54 µs. **Do not WRITE to either display before the serial link start up delay has expired.**

Start Up Time vs. CLK Frequency

CLK FREQ	Start Up Delay
9.6MHz	106.7 µs
19.2MHz	53.3 µs
30MHz	34.13 µs

OFF PHASE

In the OFF phase, differential transmitters are turned off and the lines are both driven to Ground. *Figure 7* shows the transition of the serial bus into the OFF phase. The link may be powered down by asserting Master and Slave PD* pins, the Master PD* pin alone or stopping the clock . To avoid loss of data the clock input should only be asserted after the serial bus has been in the IDLE state for at least 100 DC clock cycles. This also applies to when Master's PD* input is asserted. The 100 DC clock cycles give the Slave enough time to complete any write operations received from the serial bus.

Do not asserted the Slave PD* pin alone, as this will not reset the link properly. If the Slave PD* pin is asserted, the Master's PD* must also be asserted to generate a proper start up sequence.

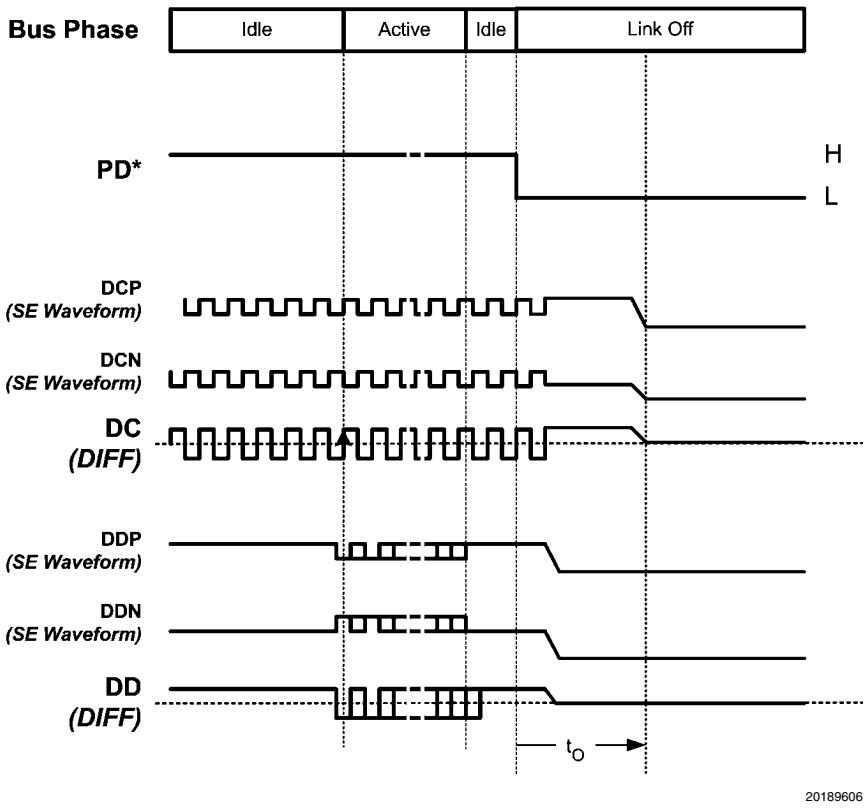


FIGURE 7. Serial Bus Power Down Timing

I80 CPU INTERFACE COMPATIBILITY

The CPU Interface mode provides compatibility between an i80 CPU Interface and a small form factor (SFF) Display or other fixed I/O port application. Both WRITE and READ transactions are supported. READs require a dual access on the Master to complete the operation.

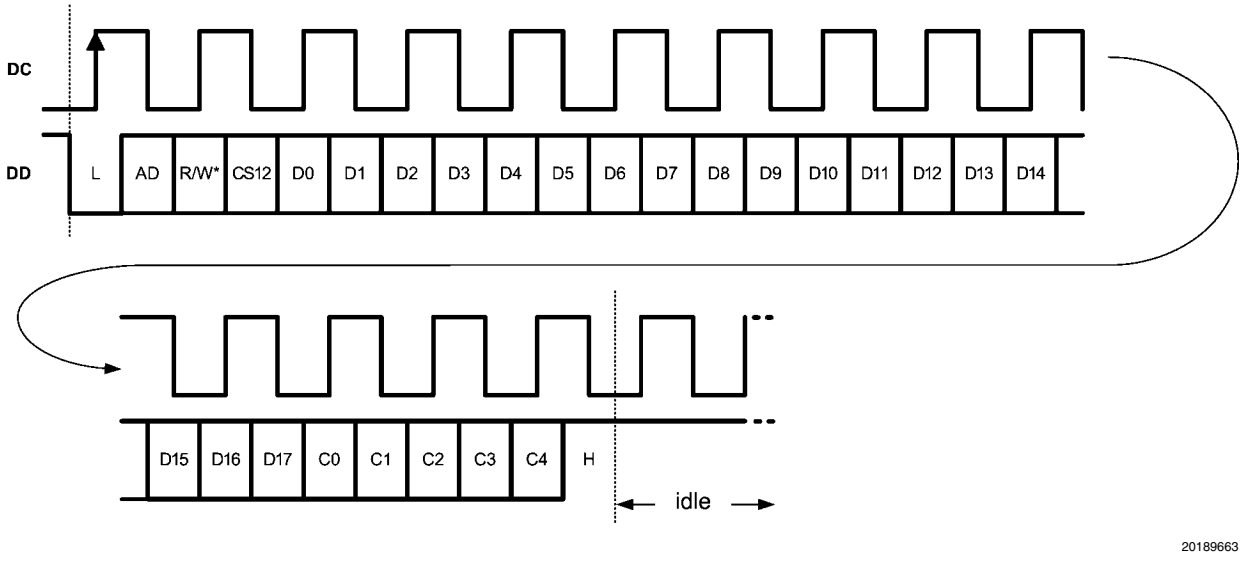


FIGURE 8. WRITE Transaction

WRITE TRANSACTION

The WRITE transaction consists of 14 DC cycles to send the control, data and CRC information on the DD signal. This includes the Start Bit, AD, R/W*, CS12, D[0:17], CRC bits C[0:4] and a reserved bit (High). See *Figure 8*. The data payload is sent least significant bit (LSB) first. The CS1/2 bit denotes which Chipset pin was active. CS1/2 = HIGH designates that CS1* is active (Low). CS1/2 = LOW designates that CS2* is active (Low). CS1* and CS2* Low is not allowed. The AD carries the information on the AD input signal. The R/W* will be Low for a Write transaction.

Figure 9 illustrates a WRITE transaction showing Master Input, SLVS, and Slave output timing. *Table 2* lists the WRITE timing parameters.

On the Master input, an i80 style WRITE is shown. The ChipSelect (CS1* or CS2*) is Low. The WR* goes Low, and Data and AD signals are sampled on the rising edge of the WR* signal. A tight set and hold window is required as shown by T1 and T2. A Latency delay later (T4) the SLVS start bit will be transmitted on the DD signal. Since it takes 14 DC cycles to send the serial word, a maximum load rate on the Master input should be slower than this (16 DC cycles or longer). This is T3 in *Figure 9*.

The Slave output timing is shown in the bottom of *Figure 9*. Note that the SLV output timing is different than the MST input timing, however the same information is conveyed. T5 is the latency delay of the Slave and also the serial payload length. Once the start bit is received, it will take this long for the SLV output to update. First, the Data[0:17], AD and CS* bits will update as required. One DC cycle later the WRITE signal will transition Low for **12** DC cycles. Then the WRITE signal will transition High and the Display will latch the data. There is a minimum hold time of one DC cycle (T9). This hold time can (will) be longer as the outputs hold their last state until the next transition is received. Also note that the CS1* and CS2* signals also hold their last state until they need to change. This would occur if a transaction is received for the other CS* signal, or if the Slave enters Power Down (PD*=L).

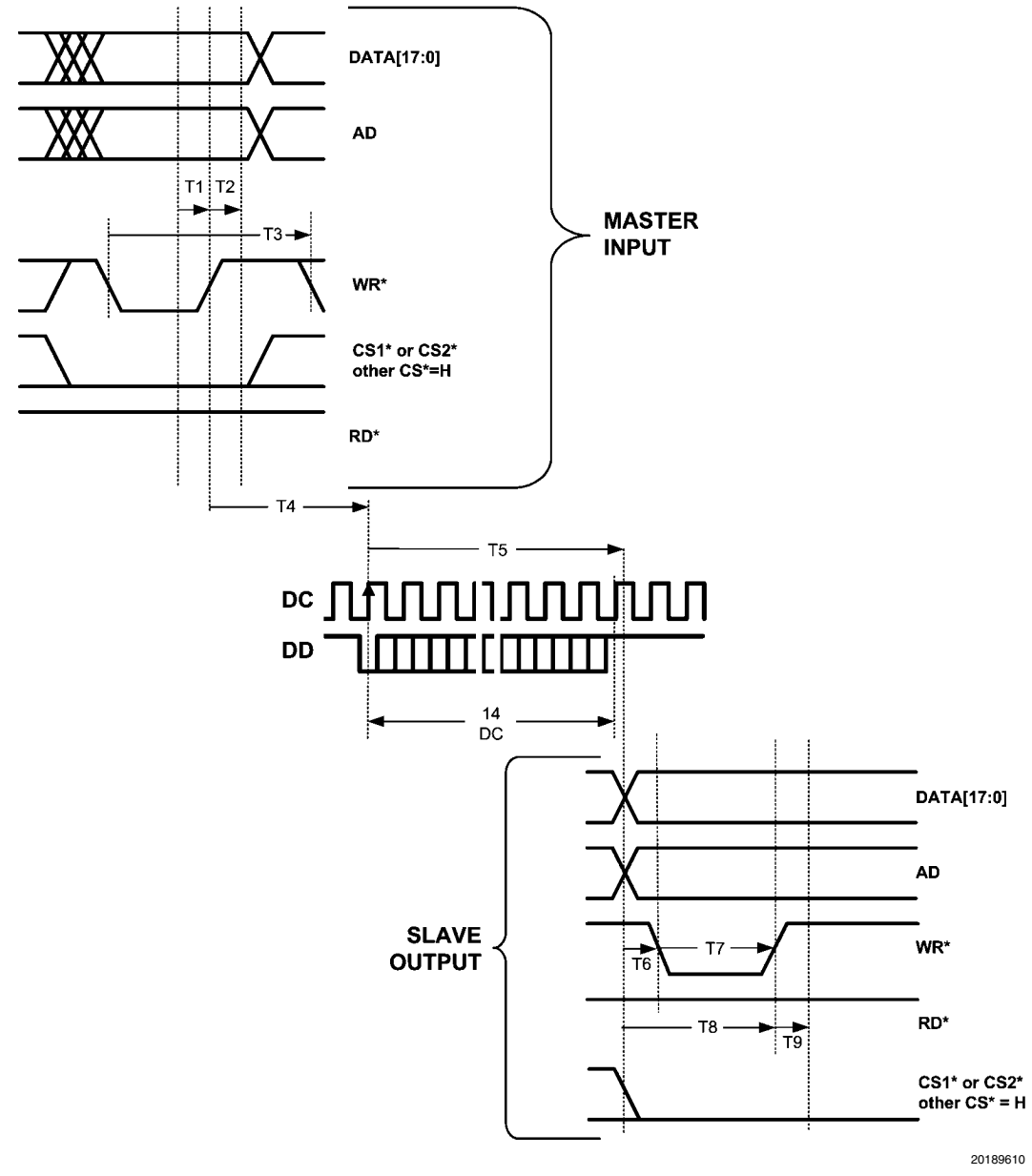


FIGURE 9. WRITE Waveforms

TABLE 2. i80 CPU WRITE Interface Parameters

No.		Parameter	Min	Typ	Max	Units
T1	MasterIN	Data and address Setup Time before Low-High Edge	5			ns
T2	MasterIN	Data and address Hold after Low-High Edge	5			ns
T3	MasterIN	Bus Cycle Rate		16		DC Cycles
T4	Master	Master Latency		7		DC Cycles
T5	Slave	Slave Latency		15		DC Cycles
T6	SlaveOUT	Data Valid before WR* High-Low		1		DC Cycles
T7	SlaveOUT	WR* Low Pulse Width		12		DC Cycles
T8	SlaveOUT	Data Valid before WR* Low-High,		13		DC Cycles
T9	SlaveOUT	Data Valid after WR* Low-High		1		DC Cycles

READ TRANSACTION

The READ transaction is similar to the WRITE but longer. The full serial READ transaction is shown in *Figure 10* . CRC bits protect both the READ command sent from the Master to the Slave (C[0:4] bits), and also the Data sent back from the Slave to the Master (RC[0:4] bits). The READ transaction consists of four sections.

In the first section the Master sends a READ Command to the Slave. This command is the same as a WRITE, but the R/W serial bit is set High and the data payload is ignored. The CRC bits are used to ensure that the transaction is valid and prevents a false READ from being entered. The Control Input "Write Only - WO" on the Slave must be set to WRITE & READ mode (Low) to support READ transactions.

In the second section (TA') the DD line is turned around, such that the Master becomes the DD Receiver and Slave becomes the DD Line Driver. The Slave will drive the DD line High after a fixed number of DC cycles. This ensures that the DD lines are a stable High state and that the High-to-Low transition of the "Start" bit is seen by the Master.

The third section consists of the transfer of the read data from the Slave to the Master. Therefore the back channel data signaling rate is ¼ of the forward channel (Master-to-Slave direction). When the Slave transmits data back to the Master, it drives the DD line Low to indicate start of read data, followed by the actual read data and CRC payload.

The fourth and final section (TA") occurs after the read data has been transferred from the Slave to the Master. In the fourth section the DD line is again turned around, such that the Master becomes the transmitter and the Slave becomes the receiver. The Slave drives the DD line High for 1 bit and then turns off. The DD lines are OFF momentarily to avoid driver contention. The Master then drives the DD line High for 1 bit time and then idles the bus until the next transaction is sent (WRITE or another READ).

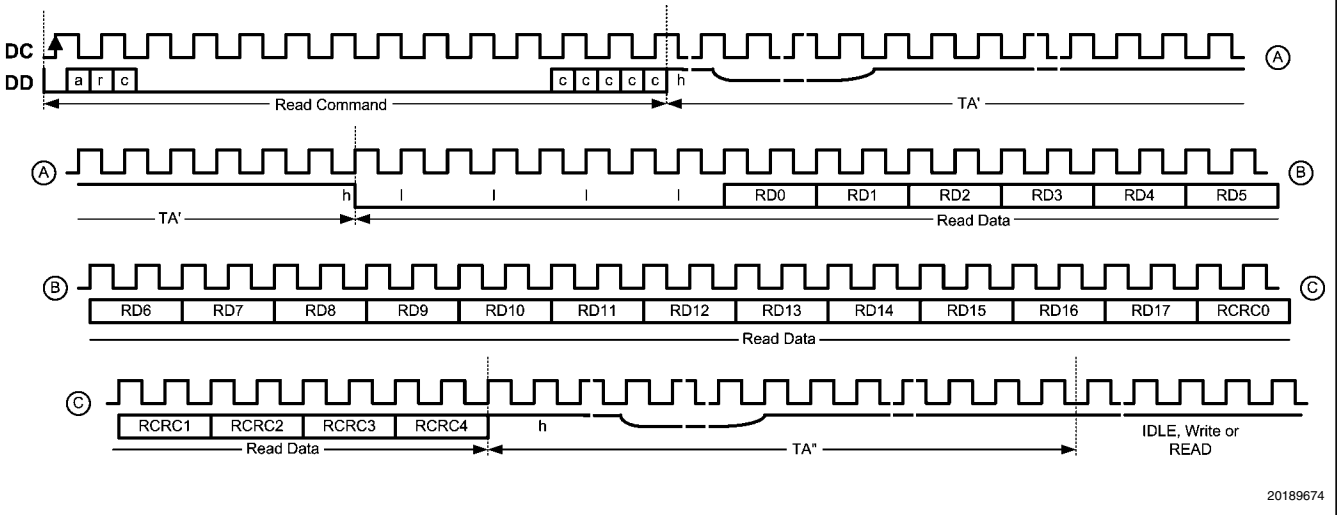


FIGURE 10. READ Transaction

The READ transaction requires a dual cycle on the Master input to complete. Once the first READ is done (RDCycle1) the serial link is busy until the second READ (RDCycle2) is done. The Host may do transactions to other devices between the READs, just not to CS1* or CS2*. On the first READ, the CS1* or CS2* line is driven low and the RD* pulses low. A fixed Data Word of all Lows is returned and should be ignored by the Host. The requested data will be available at the Master after 480 DC cycles. The second READ should now be done to collect the requested data. Upon the READ from the host, the Master will turn ON its 18 data drivers and output the data to the Host and then turn them off.

When the READ is received, the Data output buffers turn off to avoid contention. After 140 DC cycles the RD* signal switches Low. It then switches High after another 62 DC cycles and latches in the Data from the Display. The CRC is then calculated and sent to the Master. To avoid floating the inputs to the Display, the Slave data outputs are turned back on.

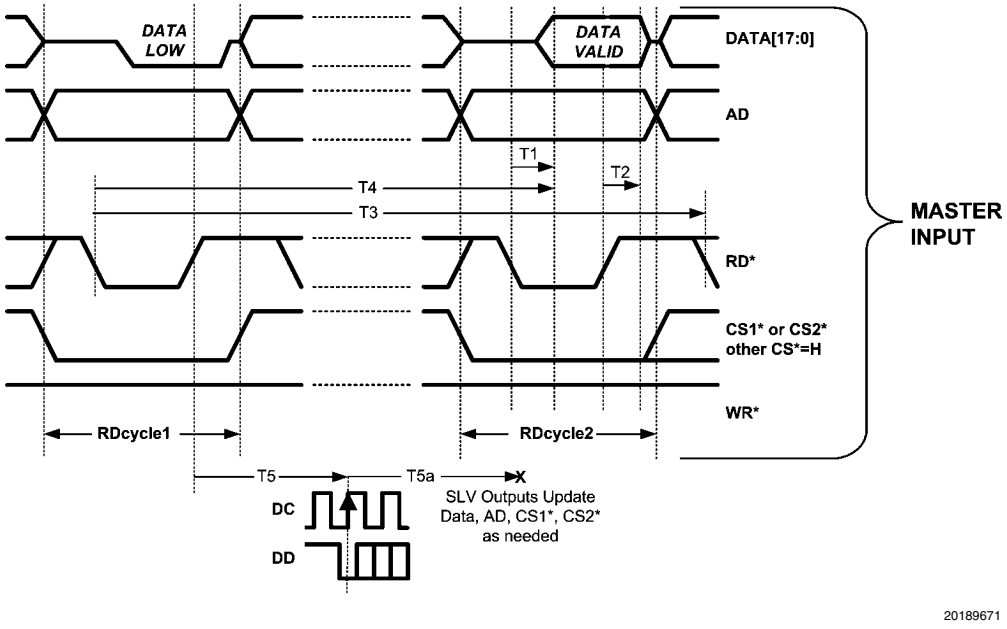


FIGURE 11. Master Input READ Timing

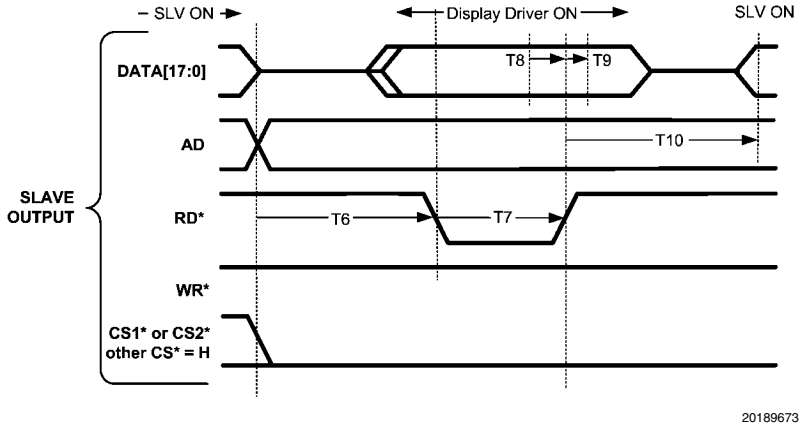


FIGURE 12. Slave Output READ Timing

TABLE 3. i80 CPU READ Interface Parameters

No.		Parameter	Min	Typ	Max	Units
T1	MasterOUT	Data and address valid after RD* High-to-Low		15		ns
T2	MasterOUT	Data and address valid after RD* Low-to-High		0		ns
T3	MasterIN	Delay Time Between READs	500			ns
T4	MasterIN	Delay Time Until Data Available (RDcyc2)	480			ns
T5	Master	Master Latency		7		DC Cycles
T5a	Slave	Slave Latency, (not shown)		158		DC Cycles
T6	Slave	AD Set Time before RD* High-to-Low		140		DC Cycles
T7	Slave	RD* Pulse Low Width		62		DC Cycles
T8	Slave	Data Set Time		7		DC Cycles
T9	Slave	Data Hold Time		0		ns
T10	Slave	Slave Data Outputs		8		DC Cycles

SLAVE OUTPUT TIMING / DISPLAY COMPATIBILITY

Compatibility of target device's timing requirements should be checked. Check that the Slave WR* active low pulse is wide enough for the target display(s). If the Slave output is too fast, a slower DC rate should be chosen (PLL setting or CLK rate may be adjusted). See **SYSTEM CONSIDERATION** section also.

Figure 13 illustrates the timing of two writes being sent to CS1*. Note that on the Slave output for Word N, that the DATA, AD, and CS signals hold their last state until the next transaction is received. This effectively extends the Hold time after Word N's WRITE rise. The length of this period (idle) is determined by the time until the next transaction on the Master input. When the second write is received (Word N+1) the Data, AD, and CS signals update as needed. Note that the active CS signal stay low until a transaction to the other CS is received or the Slave is put into powerdown.

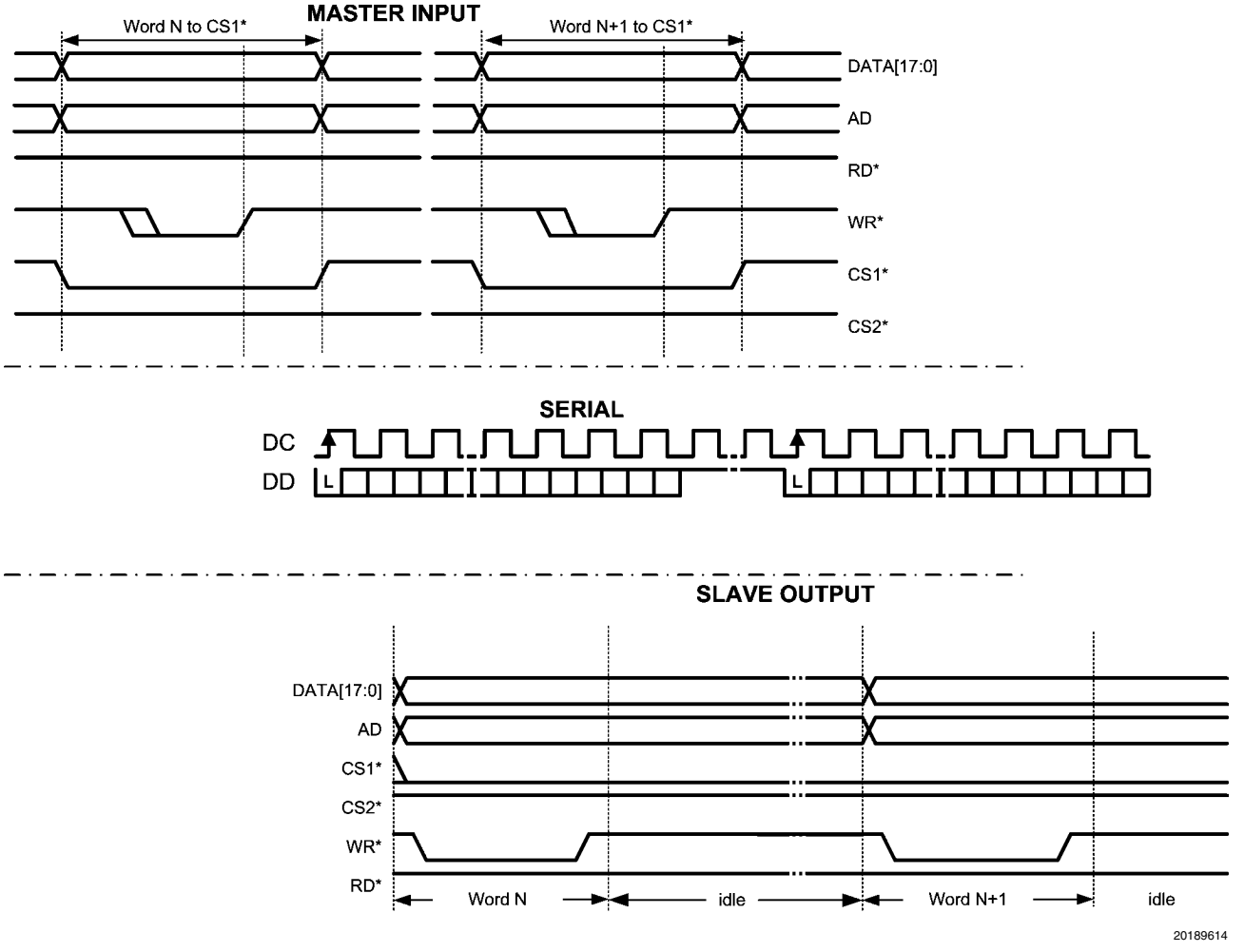


FIGURE 13. Timing Example - Two WRITEs to CS1*

CYCLIC REDUNDANCY CHECK (CRC)

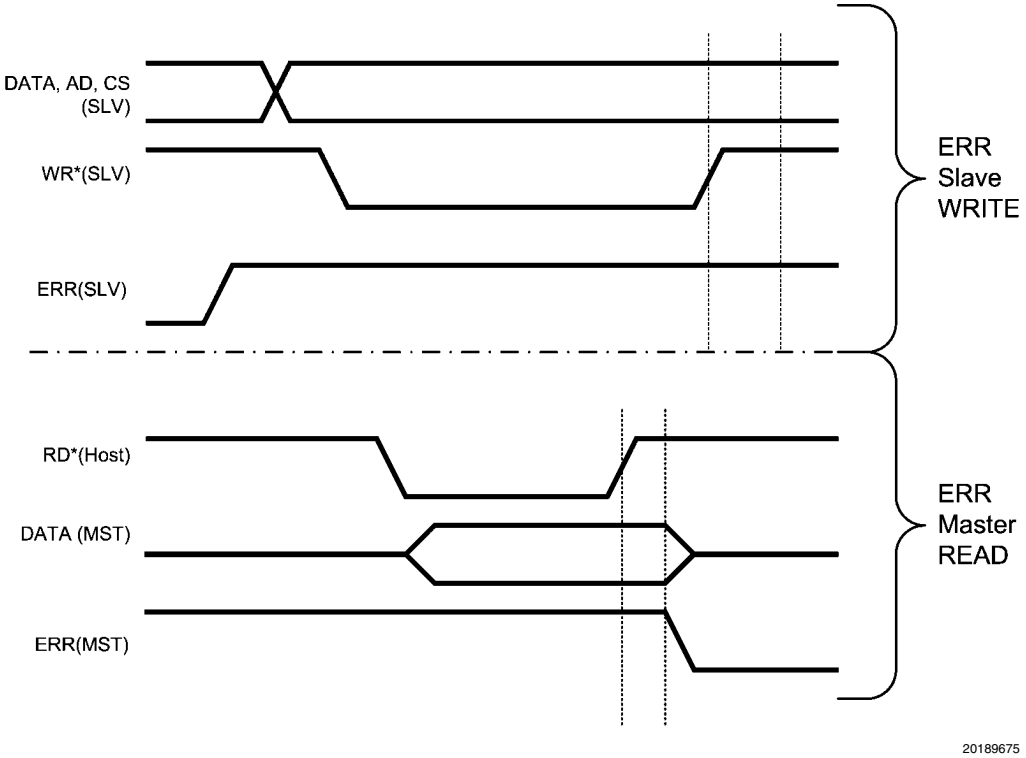
The CRC is used to detect errors in both WRITE and READ transactions on the serial link. The LM4308 uses a 5-bit CRC field to detect errors in the 22-bit payload. The Transmitting device calculates the CRC and appends it to the payload. The Receiver also calculates the CRC and compares it to the received CRC. If they are the same, the transmission is error free. If they are different, the ERR pin then flags the error.

CRC provides a better coverage than a parity bit, which can only flag one half of the possible errors. The CRC is calculated by taking the payload and adding 5 zeros and then dividing by a fixed number. The remainder of the calculation is the 5-bit CRC field that is transmitted.

If a CRC error handling is shown in the table below. See also *Figure 14*.

CRC Error Response

Operation	Direction	Error	Response
Write	Master-to-Slave	CRC error	Slave Flags, ERR pins remains High until PD* cycle or Power cycle, Data is written to the display
Read Command	Master-to-Slave	CRC error	Slave Flags, ERR pins remains High until PD* cycle or Power cycle, Slave does nothing
Write	Master-to-Slave, Slave WO = H	CRC error, Serial R/W* bit error (False Read)	Slave Flags, ERR pins remains High until PD* cycle or Power cycle, Data is written to the display (write expected)
Read Data	Slave-to-Master	CRC error	Master Flags, ERR goes High, then Low after 2nd READ, Data = X
Read Data	Slave-to-Master	Read Data not received by Master	Master times out, drives all Low data, then on 2nd READ cycle ERR goes High



1 = CS1* active which is a High, and 2 = CS2* active which is a Low

FIGURE 14. CRC - ERR Output Timing

SLVS INTERFACE

Scalable Low Voltage Signaling is the differential interface used for the physical layer of the serial (Data and Clock) signals. The differential signal is a 200mV (typ) swing with a 200mV offset from ground. This generates a ±200mV (400mVpp) across the integrated termination resistor for the receiver to recover. The receiver detects the differential signal and converts it to a LVCMOS signal. Noise picked up along the inteconnect is seen as common-mode by the receiver and rejected. The low output impedance of the line driver and of the termination network help to minimize couple noise also.

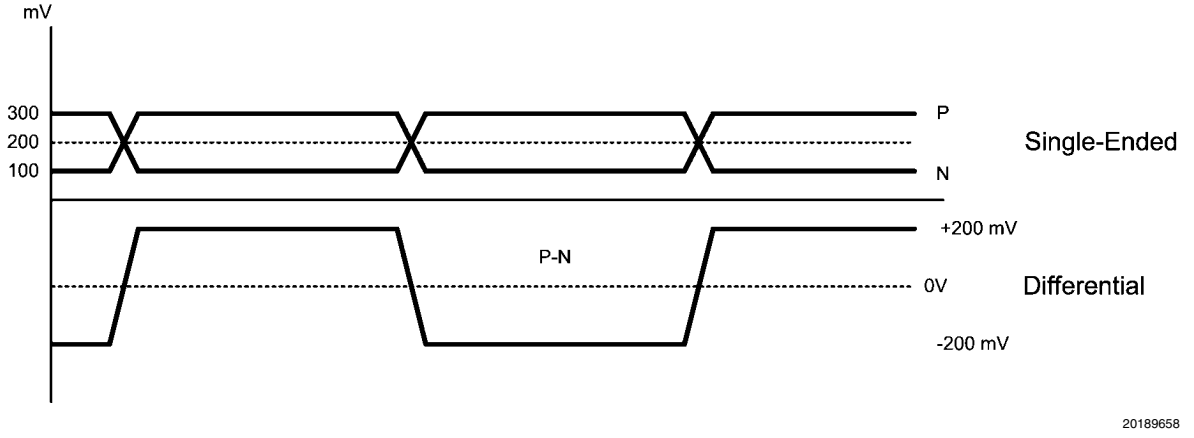


FIGURE 15. Single-ended and differential SLVS waveforms

Noise that gets coupled onto both signals, is common-mode and is rejected by the receiver. Route the traces that form the pair together (coupled) to help ensure that noise picked up is common. Differential noise that causes a dip in the signal but does not enter the threshold region is also rejected. Differntial noise margin is the minimum V_{OD} signal minus the MAX threshold voltage. 140mV - 70mV = 70mV minimum differential noise margin.

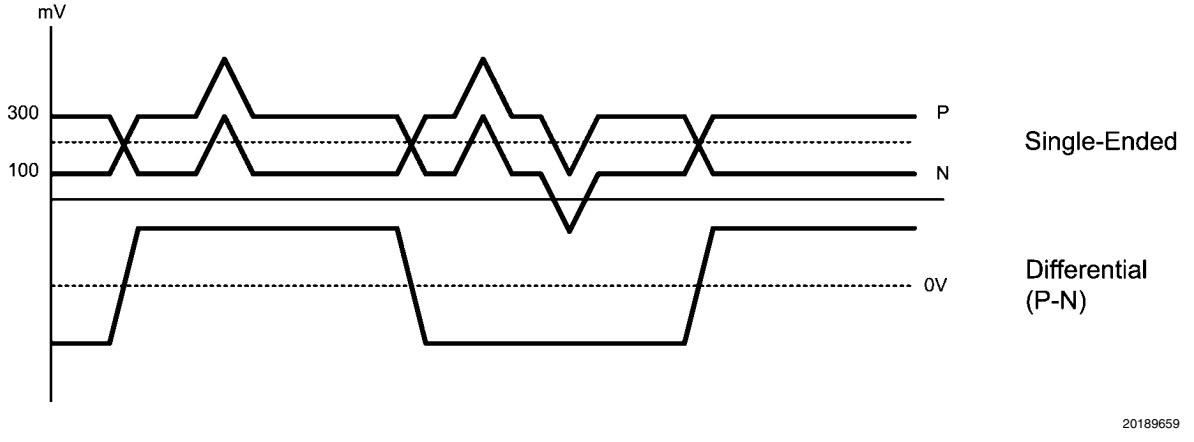


FIGURE 16. SLVS common-mode rejection waveform

LM4308 Features and Operation

POWER SUPPLIES

The V_{DD} and V_{DDA} (MPL-2 and PLL) must be connected to the same potential between 1.6V and 2.0V. V_{DDIO} powers the logic interface and may be powered between 1.6 and 3.0V to be compatible with a wide range of host and target devices.

BYPASS RECOMMENDATIONS

Bypass capacitors should be placed near the power supply pins of the device. Use high frequency ceramic (surface mount recommended) 0.1 µF capacitors. A 2.2 to 4.7 µF Tantalum capacitor is recommended near the Master V_{DDA} pin for PLL bypass. Connect bypass capacitors with wide traces and use dual or larger vias to reduce resistance and inductance of the feeds. Utilizing a thin spacing between power and ground planes will provide good high frequency bypass above the frequency range where most typical surface mount capacitors are less effective. To gain the maximum benefit from this, low inductance feed points are important. Also, adjacent signal layers can be filled to create additional capacitance. Minimize loops in the ground returns also for improved signal fidelity and lowest emissions.

MASTER / SLAVE CONFIGURATION

The LM4308 device can be configured to be a Master or a Slave with the M/S* pin. For normal modes, TM (Test Mode) input must also be Low, setting TM High enters a factory test mode.

UNUSED/OPEN LVCMOS PINS

Unused inputs must be tied to the proper input level — do not float them. Unused outputs should be left open to minimize power dissipation.

LVCMOS MASTER INPUT PINS

CPU Interface input pins (Data, AD, CS, WR, RD) accept voltages from -300mV to (V_{DDIO} + 300mV). Inputs are not High-Z with power supplies OFF. If communication between the Host (i.e. BBP) and other devices (i.e. Memory) is required when the display is not ON; the power to the Master must be ON, and the Master should be in SLEEP mode (by CLK Stop or PD*=L). In this condition, Master inputs are High Z and will not load (or clamp) the shared bus signals. Master inputs are not in a High Z state when Master V_{DDIO} = 0V.

MASTER CLOCK INPUT

The Master Clock input is a special 3.3V Tolerant input pin. This allows the clock tree to be powered from a different V_{DDIO} than the CPU interface from the host device.

PLLCON1	PLLCON0	Multiplier	CLK Range
0	0	8	9.6 to 30 MHz
0	1	10	9.6 to 24 MHz
1	0	12	9.6 to 20 MHz
1	1	Reserved	Reserved

PHASE-LOCKED LOOP

When the LM4308 is configured as a Master, a PLL is enabled to generate the serial link clock. The Phase-locked loop system generates the serial data clock at several multiples of the input clock. The DC rate is limited to 240 MHz. The PLL multiplier is set via the PLLCON[1:0] pins. Multipliers of 8X, 10X and 12X are available.

For example, if the input clock is 19.2MHz, and a 8X multiplier is selected, DC will be 153.6 MHz. and the DD line rate is 307.2 Mbps (raw bandwidth).

POWER DOWN OUTPUT STATES

When the device is in the SLEEP state (PD*=L) the output pins will be driven to the states shown in the table below.

Device	Signal	State in Power Down
Slave	Data[17:0]	Low
Slave	CS1*, CS2*, WR*, RD*, AD	High
Slave	ERR	Low
Master	ERR	Low

SLAVE

Upon application of power to the SLV device, all outputs are turned on and held in their de-asserted states.

MASTER

Upon application of power to the MST device, the ERR output is ON, and is logic low (normal mode).

SLEEP MODE OPTIONS

The Master can enter sleep mode by three options. The PD* pin is driven low, the clock input is stopped, or if the power supplies are turned off.

The simplest option is a control signal to drive the PD* input. When PD* input is driven low, the device enters a sleep mode and supply current is minimized. This mode also supports high-Z Master LVCMOS inputs. The second option is with Power ON, PD* = H, and the CLK input is stopped. The CLK stop state is recommend to be logic Low. The Master detects this state and enters the sleep state. The third option is to cut power to the device. In this configuration the LVCMOS inputs are not High-Z due to internal diodes for ESD protection.

There are also three options for the Slave to enter the sleep state. These are: based on the MPL-2 interface, the Slave PD* input pin, and by powering off the Slave device.

With power ON, and the Slave PD* input = H, the Slave detects the state on the MPL-2 bus and powers up or enters sleep mode. Direct control of the Slave is also possible by the use of its PD* input pin (relative to the Slave's V_{DDIO} levels). The third option is to turn off power to the Slave. In this configuration, do not enable and activate the Master outputs without the Slave also being ON.

SLAVE OUTPUT DRIVE STRENGTH CONTROL

The Slave Outputs have two drive strength options to support a wide range of V_{DDIO} operation. See *RDS[1:0] - Receiver Output Drive Strength*. If the SLV V_{DDIO} is 1.8V TYP, RDS0 and RDS1 should be set to a logic High. Depending upon application speed, RDS0 can be set to a logic Low to soften the edge rate on the Data signals for less noise. For high V_{DDIO} operation (i.e. 2.8V), both RDS0 and RDS1 should be set to a logic Low.

SLAVE WRITE ONLY MODE

In some applications, only WRITE operations may be required. In this case, the Slave can be configured to only support WRITE transactions by setting the WO configuration input High.

Application Information

SYSTEM CONSIDERATIONS

DUAL SMART DISPLAY APPLICATION

A Dual Smart Display application is shown in *Figure 17*. The Master (MST) resides by the host and connects to a Memory Interface. V_{DDIO} on the MST is set to be the same as the Host's port. i80 CPU Bus signals are connected as shown (Data, AD, WR*, RD*, and CS* signals). The Master also has a SLEEP mode to save power when the display is not required. The Sleep state is entered when the PD* signal is driven Low. It is also entered if the PD* signal is High and the CLK input is gated off (held at a static state). In the Sleep state, supply current into the Master is >1µA typical. In this state, (Power ON, and Sleep state), the Master inputs will not load the shared bus, and communication between the host and other devices may occur. If power is OFF (V_{DDIO} = 0V), Master input ESD diodes will clamp the bus, preventing communication on the bus. The Master requires a system clock reference which is typically 19.2MHz in CDMA applications. This signal is used to generate the serial DC clock. The CLK input is multiplied by the selected PLL multiplier to determine the serial clock rate. In the 19.2MHz CLK and 8X application, the DC rate will be 153.6MHz. Due to the serial transmission scheme using both clock edges, the raw bandwidth of a WRITE is 307.3 Mbps. The Master also provides a ERR pin that reports a CRC error on a READ transaction. The host may monitor this signal if desired, or it may be brought out to a test point only. Several configuration pins are also required to be set. For a Master, tie M/S* = H, TM = L, and PLLCON[1:0] to the desired setting.

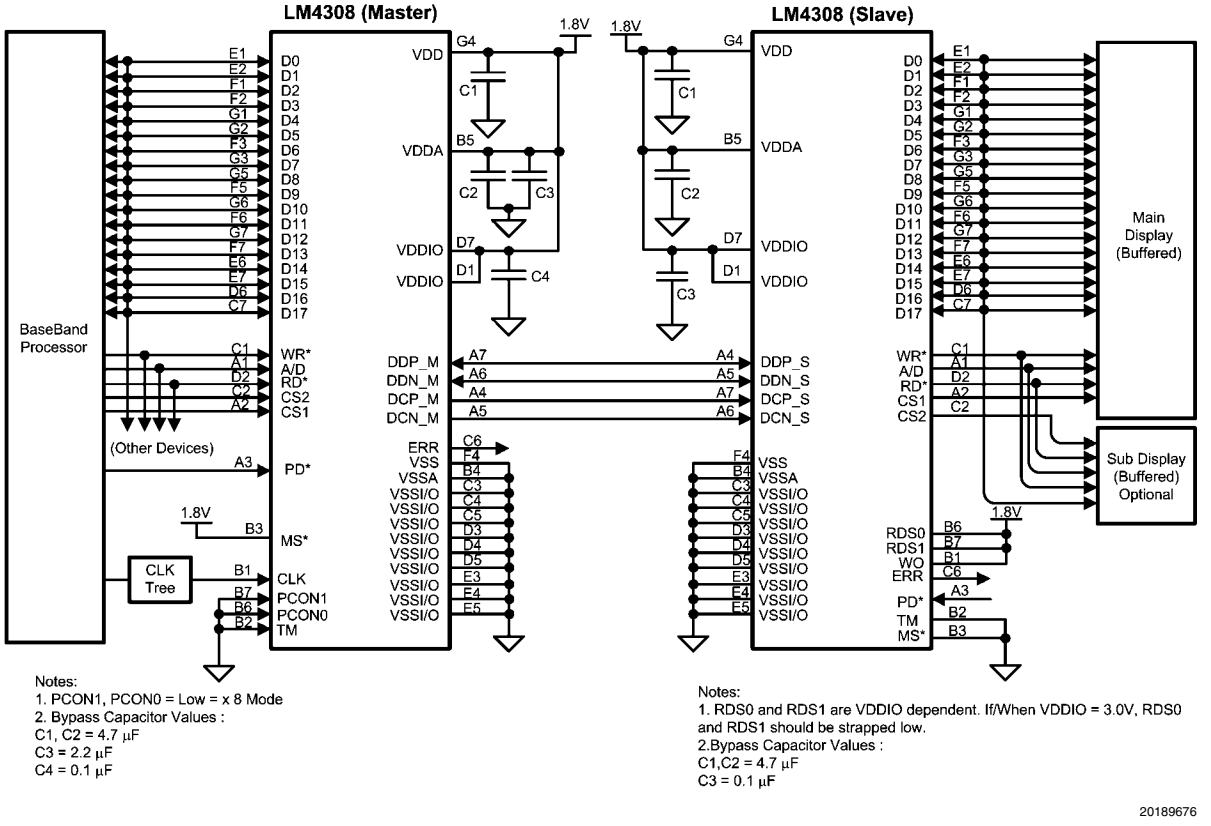


FIGURE 17. Dual SMART Display Application

The Slave recovers the serial signals and generates the parallel bus for the Display(s). The Slave V_{DDIO} is set to be compatible with the Displays employed. The Data bus signals are bidirectional to support both WRITEs and READs. The other signals. AD, WR*, RD*, and CS* signals are outputs only. The connection between the Slave device and the displays should be done such that long stubs are avoided. Extra care should be taken on the WR* and RD* signal layouts as these signals rely on the signal edges to latch the data. The Slave has user adjustable edge rate controls for the parallel bus outputs. This can be used to optimize the edge rate vs the required V_{DDIO} magnitude. Also, independent control of the strobe (WR* and RD*) is supported. This allows for the strobe signal to retain sharp edges, while using softer edges on the wide parallel data bus signals. This aids in noise reduction. The Slave also provides a ERR pin to flag any CRC errors detected. This signal maybe routed back to the host for monitoring, or bought out to a test point. The Slave supports a WRITE ONLY mode (READ operation and serial bus turn around is prevented). This mode is obtained by setting the WO pin to a logic High. The Sleep state of the display may be entered by driving the PD* signal to a logic Low. Outputs are then set to their Power Down de-asserted states. Several configuration pins are also required to be set. For a Slave, tie M/S* = L, TM = L, and WO and RDS[1:0] to the desired setting. If only one display is required in the application, the unused CS output signal should be left un-connected.

In this application, WRITEs and READs for the Displays are serialized and sent to the displays. Transaction to other devices on the shared bus (MST input) are ignored by the Master.

SYSTEM TIMING CONSIDERATIONS

When employing the SERDES chipset in place of a parallel bus, a few system considerations must be taken into account. Before sending commands (i.e. initialization commands) to the display, the SERDES must be ready to transmit data across the link. The serial link must be powered up, and the PLL must be locked. Also, a review of the Slave output timing should be completed to insure that the timing parameters provided by the Slave output meet the requirements of the LCD driver input. Specifically, pulse width on WR* and RD*, data valid time, and bus cycle rate should be reviewed and checked for display compatibility. Additional details are provided next:

The serial link should be started up as follows: The chipset should be powered. During power up, the PD* inputs should be held Low and released once power is stable and within specification and link transmission is desired.

Before data can be sent across the serial link, the link must be ready for transmission. The CLK needs to be applied to the MST, and the PLL locked. This is controlled by a keep-off counter set for 1024 CLK cycles. After the PLL has locked and the counter expired, transmission may now occur. For a 19.2MHz application is is less than 54µs delay. If a WRITE is done to the display during this time, it will be lost and the display may not be properly configured. Ensure that the **FIRST WRITE** to the display is done **AFTER** the link is ready for transmission.

It takes 14 DC Cycles to send a 18-bit CPU Write including the serial overhead. The DC cycle time is calculated based on the PLL Multiplier setting and also the input clock frequency. For example, a 19.2 MHz input CLK and a 8X PLLCON [1:0] setting yields a DC frequency of 153.6 MHz. Thus it takes ~100 ns to send the word in serial form. To allow some idle time between transmissions (this will force a bit sync per word if the gap is long enough in between), the load rate on the Master input should not be faster than 16 DC cycles, or every 105 ns (9.6 MT/s) in our example to support a data pipe line. This is sometimes referred to as the bus cycle time (time between commands). Thus the time between WRITEs on the Master Input **MUST NOT** be faster than 105 ns, otherwise the FIFO will overflow and data will be lost.

The Slave output WR* and RD* timing is a function of DC cycles alone. The width of the WR* pulse low is **TWELVE DC cycles** regardless of the pulse width applied to the Master input. In the 19.2MHz & 8X application, the WR* pulse low will be 78 ns. System designers need to check compatibility with the display driver to ensure that this pulse width meets its requirement. If it is too fast, select a lower PLL Multiplier or apply a slower input clock.

PCB LAYOUT – SERIAL SIGNALS

The LM4308 provides a swap function of SLVS DD and DC lines depending upon the state of the M/S* pin. This facilitates a straight through via-less SLVS interface design eliminating the needs for via and crossovers as shown on *Figure 18*. It is recommended to use separate logic symbols for the Master and the Slave to avoid layout errors. **NOTE THAT THE PINOUT IS DIFFERENT FOR A MASTER AND SLAVE CONFIGURED DEVICE.**

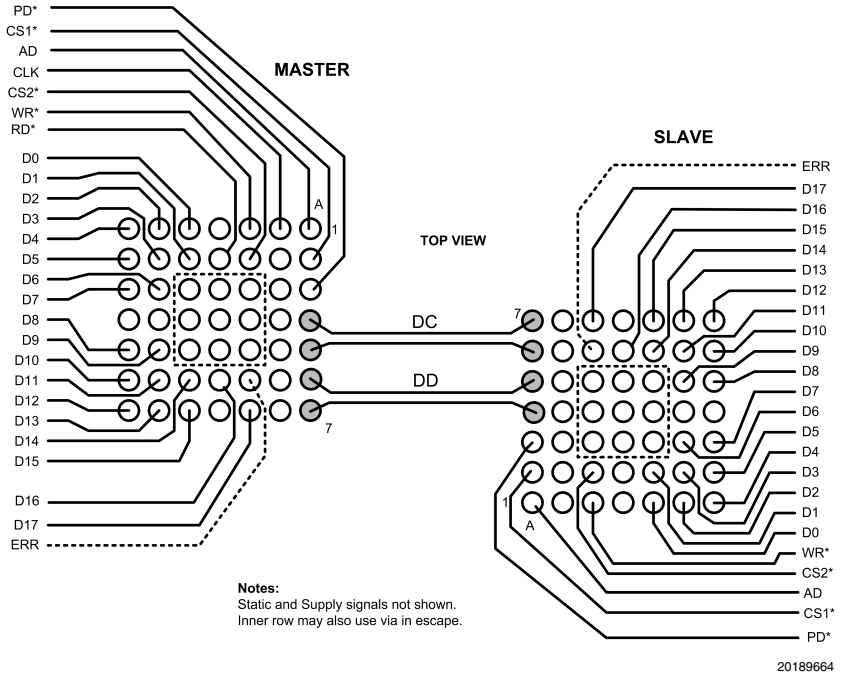


FIGURE 18. SLVS Interface Layout

FLEX CIRCUIT RECOMMENDATIONS

A differential 100 Ohm transmission path will yield the best results and be matched to the integrated differential termination resistance. Also, the interconnect should employ a coupled lines to ensure that the majority of any noise pick up is common-(equal on both the P and N signals) so that it is rejected by the differential receiver. A GSSGSSG pinout is recommended. Depending on external noise sources, shielding maybe required.

GROUNDING

Even though the serial Data and Clock signals are differential, a common ground signal is still required. This provides a common ground reference between the devices and a current return path for the common mode current.

GENERAL GUIDELINES and RECOMMENDATIONS FOR PCB DESIGN

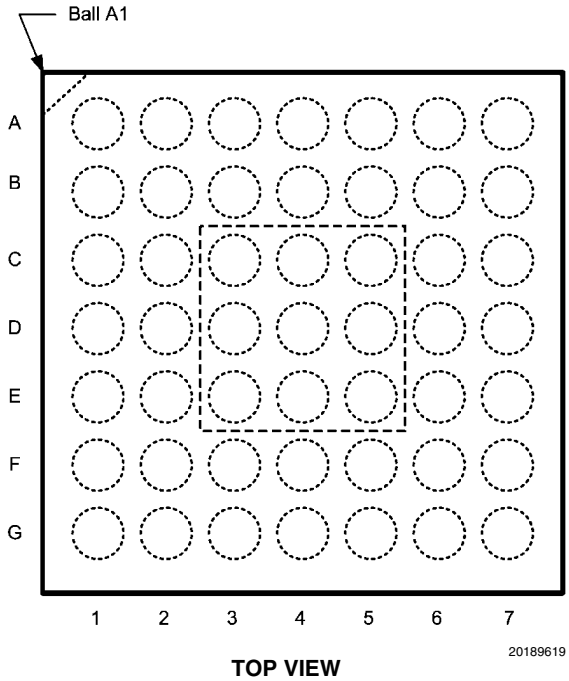
LVCOMS Signals:

- To reduce EMI, avoid parallel runs with fast edge, large LVCMOS swings.
- To reduce crosstalk allow enough space between traces. It is recommended to distance the centers of two adjacent traces at least four times the trace width. To improve design performance, lower the distance between the trace and the ground plane to under ~ 10 mils.
- Keep clock trace as straight as possible. Use arc-shaped traces as an alternative to the right-angle bends.
- Do not use multiple signal layers for clock signals.
- Do not use vias in clock transmission lines, as vias can cause impedance change and reflection.

SLVS Signals:

- Floor plan, locate Master near the connector to limit chance of cross talk to high speed serial signals.
- Use differential routing techniques. (i.e., match the lengths as well as the turns that each trace goes through)
- Keep the length of the two differential traces the same to minimize the skew and phase difference.
- Route serial traces together, minimize the number of layer changes to reduce loading.
- Use ground lines are guards to minimize any noise coupling (guarantees distance).
- Avoid using multiple vias to reduce impedance mismatch and inductance.
- Use a GSSGSSG pinout in connectors (Board to Board or ZIF).
- Bypass the device with MLC surface mount devices and thinly separated power and ground planes with low inductance feeds.
- High current returns should have a separate path with a width proportional to the amount of current carried to minimize any resulting IR effects.
- Slave device - follow similar guidelines.
- see AN-1126 (BGA) and AN-1187 (LLP) also

Connection Diagram microArray Package



TOP VIEW
(not to scale)

Note that the pinout of a MASTER configured device is DIFFERENT than a SLAVE configured device. The use of two logic symbols for PCB schematic is recommended.

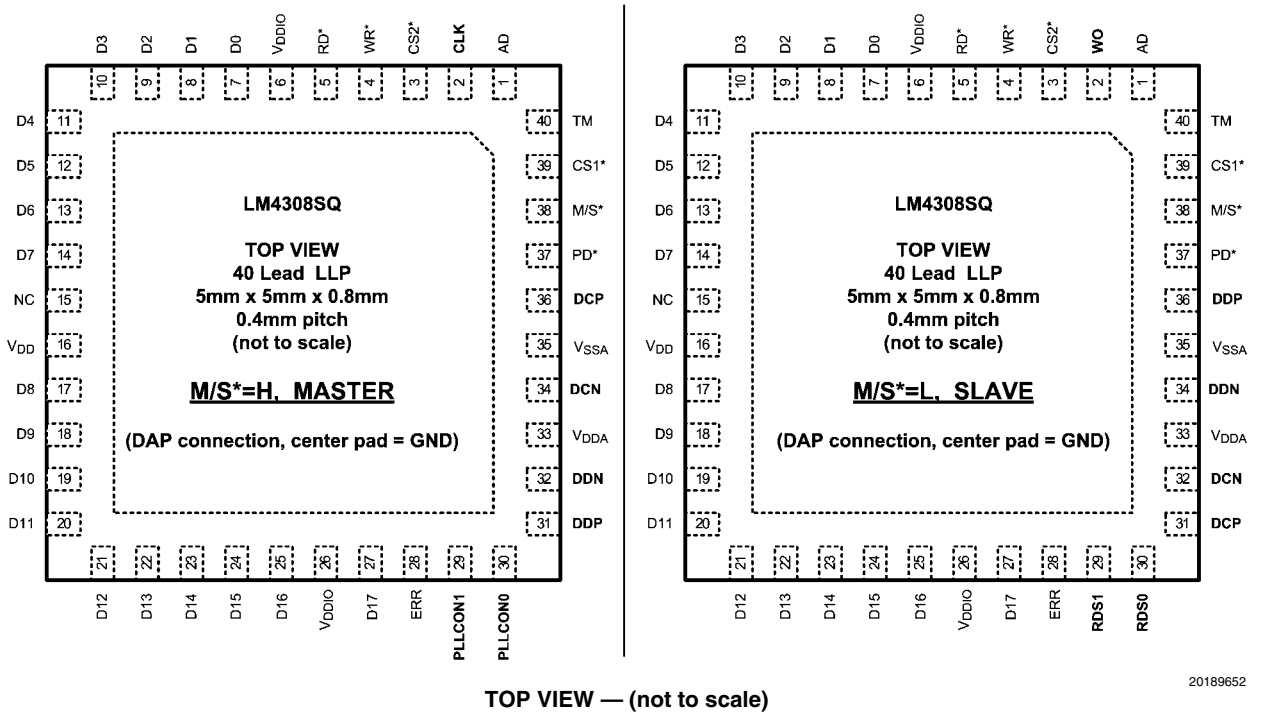
CPU Master Pinout

MST	1	2	3	4	5	6	7
A	AD	CS1*	PD*	DCP_M	DCN_M	DDN_M	DDP_M
B	CLK	TM	M/S*	V_{SSA}	V_{DDA}	PLLCON0	PLLCON1
C	WR*	CS2*	V_{SSIO}	V_{SSIO}	V_{SSIO}	ERR	D17
D	V_{DDIO}	RD*	V_{SSIO}	V_{SSIO}	V_{SSIO}	D16	V_{DDIO}
E	D0	D1	V_{SSIO}	V_{SSIO}	V_{SSIO}	D14	D15
F	D2	D3	D6	V_{SS}	D9	D11	D13
G	D4	D5	D7	V_{DD}	D8	D10	D12

CPU Slave Pinout

SLV	1	2	3	4	5	6	7
A	AD	CS1*	PD*	DDP_S	DDN_S	DCN_S	DCP_S
B	WO	TM	M/S*	V_{SSA}	V_{DDA}	RDS0	RDS1
C	WR*	CS2*	V_{SSIO}	V_{SSIO}	V_{SSIO}	ERR	D17
D	V_{DDIO}	RD*	V_{SSIO}	V_{SSIO}	V_{SSIO}	D16	V_{DDIO}
E	D0	D1	V_{SSIO}	V_{SSIO}	V_{SSIO}	D14	D15
F	D2	D3	D6	V_{SS}	D9	D11	D13
G	D4	D5	D7	V_{DD}	D8	D10	D12

Connection Diagram - LLP Package



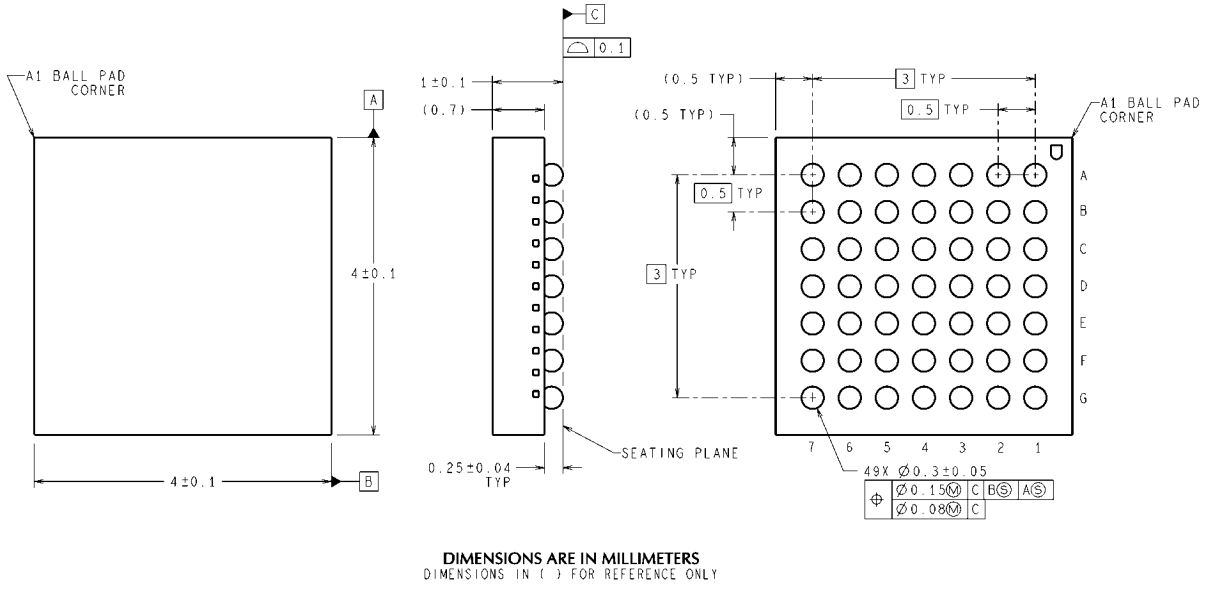
TOP VIEW — (not to scale)

Note that the pinout of a MASTER configured device is DIFFERENT than a SLAVE configured device. The use of two logic symbols for PCB schematic is recommended.

TABLE 4. CPU Master - Slave Pad Assignments

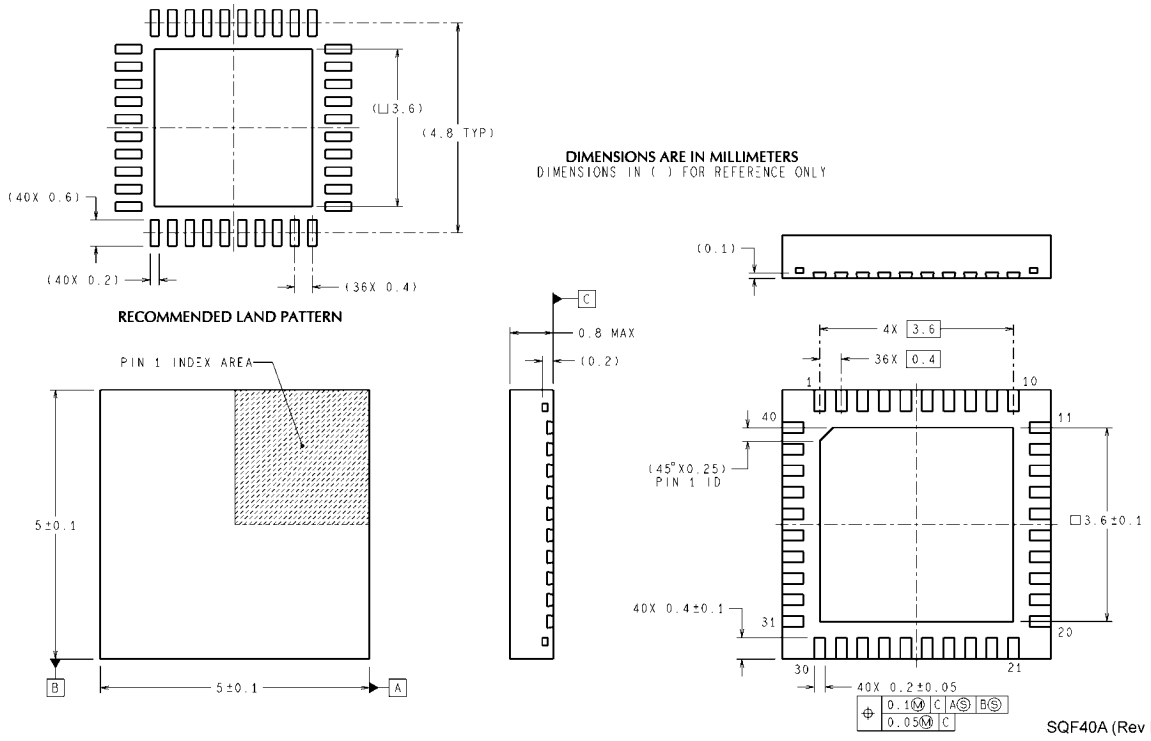
Pin #	Master	Slave		Pad #	Master	Slave
1	AD			21	D12	
2	CLK	WO		22	D13	
3	CS2*			23	D14	
4	WR*			24	D15	
5	RD*			25	D16	
6	V_{DDIO}			26	V_{DDIO}	
7	D0			27	D17	
8	D1			28	ERR	
9	D2			29	PLLCON1	RDS1
10	D3			30	PLLCON0	RDS0
11	D4			31	DDP_M	DCP_S
12	D5			32	DDN_M	DCN_S
13	D6			33	V_{DDA}	
14	D7			34	DCN_M	DDN_S
15	NC			35	V_{SSA}	
16	V_{DD}			36	DCP_M	DDP_S
17	D8			37	PD*	
18	D9			38	M/S*	
19	D10			39	CS1*	
20	D11			40	TM	
DAP	V_{SSIO} / V_{SS}			DAP	V_{SSIO} / V_{SS}	

Physical Dimensions inches (millimeters) unless otherwise noted



GRA49A (Rev A)

49L MicroArray, 0.5mm pitch
Order Number LM4308GR
NS Package Number GRA49A



SQF40A (Rev B)

40L LLP, 0.4mm pitch
Order Number LM4308SQ
NS Package Number SQF40A

Notes

Notes

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